IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Plofsky	Attorney Docket No.: ALTRP082
Application No.: Filed Herewith	Examiner: Unassigned
Filed: Filed Herewith	Group: Unassigned

Title: EMBEDDED MICROPROCESSOR FOR INTEGRATED CIRCUIT TESTING AND DEBUGGING

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service on July 29, 2003 in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR §1.10, Mailing Label Number **EV 33398 5031 US**, addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Ann Lowe

INFORMATION DISCLOSURE STATEMENT 37 CFR §§1.56 AND 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

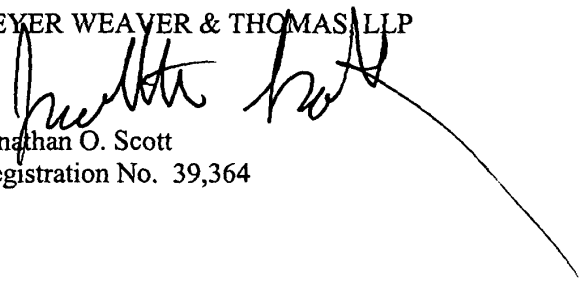
The U.S. patent(s) and U.S. published patent application(s) references listed in the attached PTO Form 1449, copies not required to be enclosed under 37 CFR 1.98 (a)(2)(1), and any and all other references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office

Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. ALTRP082).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



Jonathan O. Scott
Registration No. 39,364

P.O. Box 778
Berkeley, CA 94704-0778
(612) 252-3331

Form 1449 (Modified) **Information Disclosure Statement By Applicant** (Use Several Sheets if Necessary)	Atty Docket No. ALTRP082 Applicant: Plofsky Filing Date Filed Herewith	Application No.: Filed Herewith Group Unassigned

U.S. Patent Documents

Examine Initial	No.	Patent No. N	Date	Patentee	Class	Sub-class	Filing Date
	1	4,696,004	09/22/87	Nakajima			
	2	4,788,492	11/29/88	Schubert			
	3	4,835,736	07/11/89	Easterday			
	4	4,847,612	07/11/89	Kaplinsky			
	5	4,873,459	10/10/89	El Gamo et al.			
	6	5,036,473	07/30/91	Butts et al.			
	7	5,058,114	10/15/91	Kuboki et al.			
	8	5,329,470	07/12/94	Sample et al.			
	9	5,124,588	06/23/92	Baltus et al.			
	10	5,365,165	11/15/94	El-Ayat et al.			
	11	5,425,036	06/13/95	Liu et al.			
	12	5,452,231	09/19/95	Butts et al.			
	13	5,568,437	10/22/96	Jamal			
	14	5,572,712	11/05/96	Jamal			
	15	5,629,617	05/13/97	Uhling et al.			
	16	5,640,542	06/17/97	Whitsel et al.			
	17	5,661,662	08/26/97	Butts et al.			
	18	5,717,695	02/10/98	Manela et al.			
	19	5,717,699	02/10/98	Haag et al.			
	20	5,764,079	06/98/98	Patel et al.			
	21	5,821,771	10/13/98	Patel et al.			
	22	5,870,410	02/09/99	Norman et al.			
	23	5,960,191	09/28/99	Sample et al.			
	24	5,983,277	11/09/99	Heile et al.			
	25	6,14,334	01/11/00	Patel et al.			
	26	6,016,563	01/18/00	Fleisher			
	27	6,020,758	02/01/00	Patel et al.			
	28	6,104,211	08/15/00	Alfke			
	29	6,157,210	12/05/00	Zaveri et al.			
	30	6,182,247	01/30/01	Herrmann et al.			
	31	6,212,650	04/03/01	Alfke			
	32	6,223,148	04/24/01	Stewart et al.			

Examiner Initial	No.	Patent No. N	Date	Patentee	Class	Sub-class	Filing Date
	33	6,247,147	06/12/01	Beenstra et al.			
	34	6,286,114	09/04/01	Veenstra et al.			
	35	6,317,860	11/13/01	Heile			
	36	6,321,369	11/20/01	Heile et al.			
	37	6,389,558	05/14/02	Herrmann et al.			
	38	6,460,148	01/10/02	Veenstra et al.			
	39	6,259,271	07/10/01	Couts-Martin et al.			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	A	4042262	07/1992	DE				

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	1	Marantz, Joshua, "Enhanced Visibility and Performance in Functional Verification by Reconstruction", Proceedings of the 35th Annual Conference on Design Automation Conference, Pgs. 164-169. 1998.
	2	Stroud, Charles et al., "Evaluation of FPGA Resources for Built-in Self-test of Programmable Logic Blocks", Proceedings of the 1996 ACM 4th International Symposium on Field-programmable Gate Arrays, Pg. 107. 1996.
	3	Collins, Robert R., "Overview of Pentium Probe Mode", (www.x86.org/ariticles/problemd/ProbeMode.htm), August 21, 1998, 3 pgs.
	4	Collins, Robert R., "ICE Mode and the Pentium Processor", (www.x86.org/ddj/Nov97/Nov97.htm), August 21, 1986, 6 Pgs.
	5	"PentiumPro Family Developer's Manual", Volum 1: Specifications, Intel®Corporation, 1996, 9 Pgs.
	6	"Pentium® Processor User's Manual", Volume 1, Intel®Corporation, 1993, Pgs. 3-11.
	7	Xilinx, Inc.; ISE Logic Design Tools: ChipScope

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	8	Synplicity, Inc. "Identify™RTL Debugger" 2003; Pg 1-2.
	9	Altera, "SignalTap Analysis in the Quartus II Software Version 2.0; September 2002, ver. 2.1; Altera Corporation.
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.